UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/500,064	05/09/2005	Wolfgang Buhr	DE01 0359	7154

65913 7590 08/14/2007

NXP, B.V.
NXP INTELLECTUAL PROPERTY DEPARTMENT
M/S41-SJ
1109 MCKAY DRIVE
SAN JOSE, CA 95131

EXAMINER	
STEVENS, THOMAS H	

ART UNIT	PAPER NUMBER
2121	

NOTIFICATION DATE	DELIVERY MODE
08/14/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/500,064	BUHR ET AL.	
	Examiner	Art Unit	
	Thomas H. Stevens	2121	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05/22/2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,5-9 and 12-15* is/are rejected.

7)☒ Claim(s) *2,4,10 and 11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-15 were examined.

Section I: Final Rejection

Claim Objections

2. Claims 2, 4, 10 and 11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1,3,5-9,12-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Younger (US Patent 4,874,935; Younger). Younger teaches a smart card including a microcomputer (abstract).

Claim 1. A method for writing (column 6, lines 51-55) a data value ("non-volatile data. Data files" which consume data, column 3, lines 60-66) to a location within non-volatile (NV) memory (column 3, lines 60-63) of a smart card (abstract), the smart card (abstract) having a processor that is adapted to read (column 6, lines 51-55) from and write (column 6, lines 51-55) to the NV memory, (column 3, lines 60-63) the method comprising: providing an instruction to the processor of the smart card (abstract), the

instruction containing the data value ("non-volatile data. Data files" which consume data, column 3, lines 60-66) and an address pointer (column 6, lines 20-22) that identifies the location within the NV memory (column 3, lines 60-63); and using the processor, writing (column 6, lines 51-55) the data value ("non-volatile data. Data files" which consume data, column 3, lines 60-66) to the location within the NV memory (column 3, lines 60-63) identified by the address pointer (column 6, lines 20-22).

Claim 3. A method as claimed in claim 2, characterized in that the additional instructions of the processor perform a transfer of parameters for the address pointer (column 6, lines 20-22) and for the data value ("non-volatile data. Data files" which consume data, column 3, lines 60-66) to be written and activate corresponding control signals for a memory management unit (MMU (COLUMN 5, LINES 13-15)) and NV memory (column 3, lines 60-63) interfaces.

Claim 5. A method as claimed in claim 3, characterized in that the MMU (COLUMN 5, LINES 13-15) is extended by a control signal path ("smart card control program", column 5, lines 13-14) in the presence of a memory management unit (MMU (COLUMN 5, LINES 13-15)) of the processor.

Claim 6. A method as claimed in claim 1, characterized in that, in the presence of an MMU (COLUMN 5, LINES 13-15), only address areas of the NV memory (column 3, lines 60-63) are written to which have been enabled by the MMU (COLUMN 5, LINES 13-15).

Claim 7. A method as claimed in claim 1, characterized in that special mapping (specialized mapping, column 10, lines 20-45) of code memory is taken into account within the an address area of the processor in the presence of an MMU (COLUMN 5, LINES 13-15).

Claim 8. A method as claimed in claim 1, characterized in that a plurality of data values with a same page address are written in succession (well known with memory addressing or mapping; specialized mapping, column 10, lines 20-45).

Claim 9. A method as claimed in claim 1, characterized in that file cement of a cache page register is programmed into the NV memory (column 3, lines 60-63) by writing (column 6, lines 51-55) to a control register of the NV memory (column 3, lines 60-63).

Claim 12. A smart card (abstract) comprising: non-volatile (NV) memory; an input/output for receiving an instruction, the instruction containing a data value ("non-volatile data. Data files" which consume data, column 3, lines 60-66) to be written to a location within the NV memory (column 3, lines 60-63) and an address pointer (column 6, lines 20-22) that identifies the location; and a processor that is adapted to write (column 6, lines 51-55) the data value ("non-volatile data. Data files" which consume data, column 3, lines 60-66) to the location within the NV memory (column 3, lines 60-63) identified by the address pointer (column 6, lines 20-22) in response to the instruction, the processor further adapted to read (column 6, lines 51-55) from the NV memory.

Claim 13. A smart card (abstract) as claimed in claim 12, characterized in that the processor is adapted to write (column 6, lines 51-55) the data value ("non-volatile data. Data files" which consume data, column 3, lines 60-66) to the location within the NV memory (column 3, lines 60-63) by writing (column 6, lines 51-55) the data value ("non-volatile data. Data files" which consume data, column 3, lines 60-66) to a control register of the NV memory (column 3, lines 60-63).

Claim 14. A computer program product which comprises a computer-read (column 6, lines 51-55) able storage medium, on which a program is stored which, once it has been loaded into memory of a computer or smart card (abstract) processor, allows the computer or smart card (abstract) processor to perform writing (column 6, lines 51-55) to NV memory (column 3, lines 60-63) in a smart card (abstract), wherein is written to a location within the NV memory (column 3, lines 60-63) that is identified by an address pointer, by writing (column 6, lines 51-55) the data value ("non-volatile data. Data files" which consume data, column 3, lines 60-66) to a cache page register of the NV memory (column 3, lines 60-63) and updating page address pointer (column 6, lines 20-22) registers of the NV memory, the data value ("non-volatile data. Data files" which consume data, column 3, lines 60-66) and the address pointer (column 6, lines 20-22) contained in an instruction.

Claim 15. A smart card (abstract) comprising: non-volatile (NV) memory (column 3, lines 60-63) means; means for receiving an instruction, the instruction containing a data value ("non-volatile data. Data files" which consume data, column 3, lines 60-66) to be written to a location within the NV memory (column 3, lines 60-63) and an address

pointer (column 6, lines 20-22) that identifies the location; and a processor means that is adapted to write (column 6, lines 51-55) the data value ("non-volatile data. Data files" which consume data, column 3, lines 60-66) to the location within the NV memory (column 3, lines 60-63) identified by the address pointer (column 6, lines 20-22) in response to the instruction, the processor means further adapted to read (column 6, lines 51-55) from the NV memory (column 3, lines 60-63).

Section II: Response to Arguments

Specification

5. Applicants are thanked for addressing this issue. Objection is withdrawn.

102(b)/103(a)

6. Applicants' arguments, see pages 6-8, filed 05/22/2007, with respect to the rejection(s) of claim(s)1-12,14-15 and 12 under 35 U.S.C. 102(b) and 103(a), respectively have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Younger.

Conclusion

7. Applicants' amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

The prior art made of record and not relied upon is considered pertinent to applicants' disclosure:

- US Patent 5,377,343 teaches a security circuit for protecting data stored in an internal memory of a microcomputer has a first memory for storing an externally applied security code and a latch circuit for latching a key code in order to read data stored in the internal memory.

- US Patent 6,292,874 teaches a memory management unit is disclosed for a single-chip data processing circuit, such as a smart card.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mr. Tom Stevens whose telephone number is 571-272-3715.

If attempts to reach the examiner by telephone are unsuccessful, please contact examiner's supervisor Mr. Anthony Knight 571-272-3687. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov.. Answers to questions regarding access to the Private PAIR system, contact the Electronic Business Center (EBC) (toll-free (866-217-9197)).

Anthony Knight
Supervisory Patent Examiner
Tech Center 2100